ABSTRACT OF THE DISCLOSURE

POROUS LOW-K DIELECTRIC INTERCONNECTS WITH IMPROVED ADHESION PRODUCED BY PARTIAL BURNOUT OF SURFACE POROGENS

An electrical interconnect structure on a substrate, includes a first porous dielectric layer with surface region from which a porogen has been removed; and an etch stop layer disposed upon the first porous dielectric layer so that the etch stop layer extends to partially fill pores in the surface region of the first porous dielectric layer from which the porogen has been removed, thus improving adhesion during subsequent processing. The porogen may be removed from the surface region by heating, and in particular by hot plate baking. A second porous dielectric layer, which may have the same composition as the first porous dielectric layer, may be formed over the etch stop layer. Electrical vias and lines may be formed in the first and second porous dielectric layer, respectively. The layers may be part of a multilayer stack, wherein all of the layers are cured simultaneously in a spin application tool porous dielectric layer.